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Analysis and implementation of high step-up SEPIC converter without a coupled inductor for high voltage applications

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Abstract

In this paper, to convert the voltage of green energy sources and overcome their low output voltage problem, a high step-up interleaved SEPIC converter without a coupled-inductor is suggested. The converter introduces various advantages, which can aid in reducing the voltage stress on the converter switches and providing zero current switching conditions for all switches and diodes. Also, the control system's operation is not complicated, and due to not using a coupled-inductor, the converter's input current ripple is low, increasing the solar cell's or fuel cell's lifetime. The analysis of the converter and design procedure are stated. The converter is simulated in the PSpice software, and to prove the correctness of the analysis, a prototype of the converter has been made in the laboratory. The experimental results of the prototype confirm the theoretical analysis of the converter.

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1. Introduction

With the increase in energy consumption along with the limitation of fossil fuels and the ecological pollution produced by their consumption, finding a suitable alternative for non-renewable energy has become very important. Much research has been done in connection with renewable energies [1,2]. Utilization of wind energy, fuel cells [3,4], solar cells [5,6], and heat-to-electricity generators [7,8] are some of the most important methods for electricity production.

The wide usage of green energies is the main motive for using interface converters to increase voltage levels and power control [9,10]. Boost converters have many problems, such as switch and diode voltage pressure, high current stress on the diode, and high conduction and switching losses [11,12]. Isolated converters use transformers to increase the voltage conversion factor [13,14]. However, the weight, volume, loss, and input current ripple increases as a result of the presence of the transformer [15,16]. So, if there is no need for the photovoltaic systems to be isolated, transformer non-isolated ones are more suitable [17,18]. In non-isolated converters, methods such as coupling inductors [19], switched capacitors [20], switching at zero voltage [21], and circuits Multipliers [22,23] or a mixture of the above methods [24] are very suitable for increasing the gain and decreasing the voltage stress on the switch [25,26].

The single-ended primary inductor converter (SEPIC) is a type of DC-DC converter where the converter's output voltage can be greater, less, or equal to the input voltage. In this converter, the PWM signal controls the duty cycle of the switch. The SEPIC circuit is a mixture of a boost converter and an inverse buck-boost converter whose output voltage is not reversed; in other words, the output voltage will be in the same direction as the input voltage [27]. As a result, this converter can be utilized for voltage adjustment while maintaining a constant output voltage [28,29]. It exhibits superior efficiency compared to high static gain DC/DC converters and reduces voltage stress on all semiconductors. SEPIC converters are commonly employed in various applications, such as renewable energy systems like photovoltaic and fuel cells, battery chargers, high power factor rectifiers, light emitting diode drivers, and bidirectional DC high conversion factor systems [30,31]. Furthermore, SEPIC converters are employed to enhance the performance of different applications, such as reducing torque waves in sensorless brushless DC motor control [32], designing UPS charging systems with single-stage power factor correction [33], and enabling power conversion at high and very high frequencies [34].

It is important to note that SEPIC converters need to operate at high frequency in order to achieve low volume and fast transient response. However, an increase in the switching frequency leads to an increase in the switching losses due to the overlapping of the switch current and voltage. [35].

The utilization of an interleaved structure in high step-up converters has proven to be effective in enhancing power levels, reducing input current ripple, minimizing passive element size, and improving the transient response of the system [36]. However, conventional interleaved converters still face challenges such as reverse recovery of output diodes and high switching losses, which reduces converter efficiency [37].

Various soft switching techniques have been proposed to address these issues, including the use of active clamp auxiliary circuits, which not only help the main and auxiliary switches operate under ZVS conditions but also solve the problem of reverse recovery of output diodes [38]. Nevertheless, these converters have drawbacks such as high circulating current, duty cycle losses, and high voltage stress on switches.

Naji-Esfahani et al. investigated the closed-loop stability of the SEPIC converter using a proportional-integral-derivative (PID) controller, with model parameters adjusted using the gray wolf multi-objective algorithm [39]. They also employed the state space average method to model and determine the system's transfer function, and the stability of the system was evaluated using performance parameters such as overshoot percentage, peak time, and settling time.

Furthermore, [40] proposed a hybrid boost-SEPIC converter with soft switching for high-voltage gain applications. In that circuit, the output of the SEPIC converter was connected in series with the boost converter's output. Additionally, a coupled-inductor was used in the boost converter, leading to further benefits, and the main switch was turned on under zero current switching (ZCS) without any extra switches.

Several approaches have been proposed to enhance the voltage gain, including various methods such as coupled inductors [41], switched capacitors [42], or a combination of both [43], and the utilization of coupled inductors with lifting capacitors [44]. However, the use of coupled inductors presents inherent issues, including an increase in circuit weight, cost, input current ripple, and unwanted spikes on the switch due to leakage inductance. Thus, an alternative approach that avoids coupled inductors and reduces the number of elements would be more cost-effective, resulting in lower input current ripple.

The main structure of this paper is organized as follows: In Section 2, the proposed step-up converter schematic and its various performance states, along with calculations for voltage gain and voltage stress on converter elements, are presented. Section 3 outlines the relationships for calculating the values of passive elements and converter capacitors. Section 4 describes the simulation of the converter using PSPICE, and the corresponding simulation results are presented. Section 5 includes the experimental implementation of the converter in a laboratory, along with the obtained results that validate the correctness of the converter design. Finally, the conclusion is provided in Section 6, along with suggestions for future research directions.

2. The proposed step-up converter

Figure 1 illustrates the schematic of the proposed step-up converter, which consists of two switches, S_1 and S_2, that operate in synchronization. The control of the converter is achieved through the pulse width modulation (PWM) method, ensuring a simplified implementation of the control circuit. The converter also employs three inductors, L_1, L_2, and L_3, as well as two voltage-lifting capacitors, C_1 and C_2. To regulate the output voltage ripple, an output capacitor, C_o, and diodes, D and D_o, are utilized for efficient energy transfer.

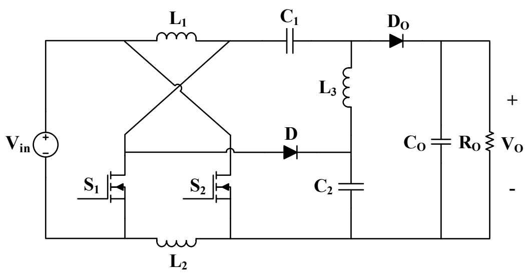


Fig1. Schematic of the proposed high-amplification SPEC converter.

2.1. Converter operation modes

The suggested converter operates in three different states within one switching cycle, as illustrated in Figure 2. For ease of performance analysis, it is assumed that the currents of inductors L_1, L_2, and L_3, as well as the voltages of capacitors Co and C, remain constant during the cycle. Additionally, L_1 and L_2 are assumed to be equal in value. The performance states of the converter are shown in Figure 3 and are described as follows:

a) First state - This state begins with switches S_1 and S_2 turning on under zero-current (ZC) switching conditions. As a result, inductors L_1 and L_2 are linearly charged with a slope of vin/L. Inductor L_3 is charged through capacitors C_2 and C_1, as well as switch S_1. The current slope of inductor L_3 is equal to $(v_{c2}-v_{c1})/L_a$ and charges linearly due to the constant voltage of C_1 and C_2. During this state, the capacitor Co supplies the output current.

b) Second state - Do and D are on immediately after the first state. L_1 and L_2 are discharged to the output through diodes Do and D, respectively. Capacitor C_2 is charged through diode D, while inductor L_3 is discharged through diode D_o to the output.

c) Third state - In this state, diode D is turned off under ZC conditions, causing a decrease in the voltage of the switches. Capacitors C_1 and C_2 are discharged and charged by inductors L_1 and L_2, respectively. The charging and discharging of the capacitors are also linear due to the constant current of the inductors. This state continues until the switches are turned on again.

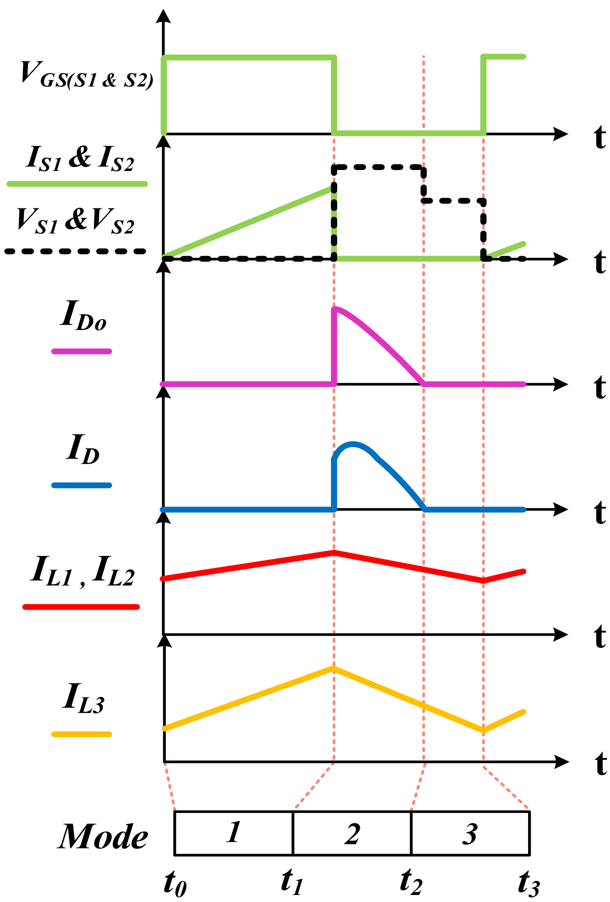
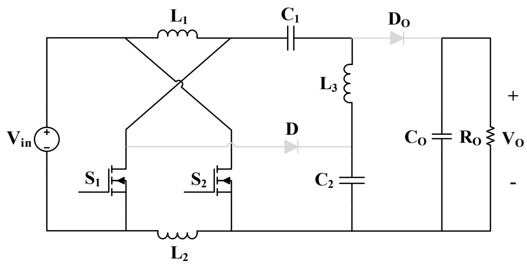
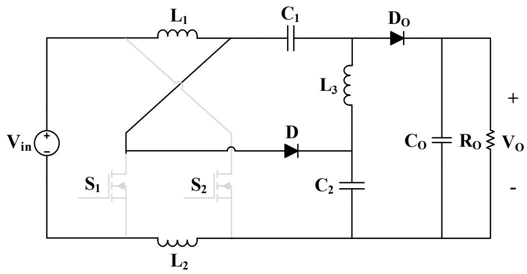


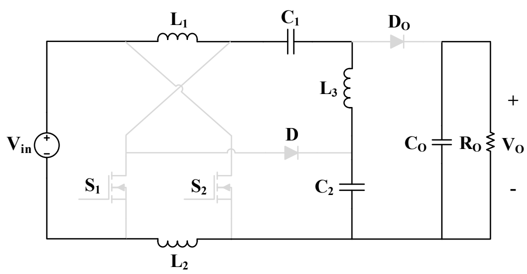
Fig 2. Key waveforms of the proposed high step-up SEPIC converter.



(a) First mode (to<t<t1)



(b) Second mode (t1<t<t2)



(c) Third mode (t2<t<t3)

Fig3. Equivalent circuit of the operational states of the proposed SEPIC converter.

2.2. Converter gain

The C_1 and C_2 voltages are determined by writing the volt-second balance for L_1 and L_3. When the switches are off, the following equations are obtained:

$$V_{L1}=V_{L2}=\frac{v_{in}-V_o+v_{C1}}{2} \quad (1)$$

$$V_{L3}=-V_{C1} \quad (2)$$

and when the switches are on, the following two equations will be present:

$$V_{L1} = V_C = V_{in} \tag{3}$$

$$V_{L3} = V_{C2} - V_{C1} + V_{in} \tag{4}$$

Therefore, by writing high-volt seconds, the voltage of capacitors C_1 and C_2 is equal to:

$$V_{C1} = \frac{2D}{1-D} V_{in} \tag{5}$$

$$V_{C2} = \frac{1+D}{1-D} V_{in} \tag{6}$$

By writing KVL in the input loop, the converter's gain is calculated according to Eq. 7. Fig. 4 shows the gain of the converter in terms of duty cycle variation.

$$M = \frac{V_o}{V_{in}} = \frac{1+3D}{1-D} \tag{7}$$

2.3. **Voltage stress of elements**

KVL must be written in the circuit loop to calculate the element's voltage stress, including the element when the element is off. Therefore, the switches' and diodes' voltage stress is obtained from the following equations. Fig. 5 shows the normalized stress diagram of the semiconductor elements of the proposed high-gain SEPIC converter.

$$V_{S1} = V_{S2} = \frac{V_{in}}{1-D} = \frac{V_o}{1+3D} \tag{8}$$

$$V_D = V_{Do} = \frac{2V_{in}}{1-D} = \frac{2V_o}{1+3D} \tag{9}$$

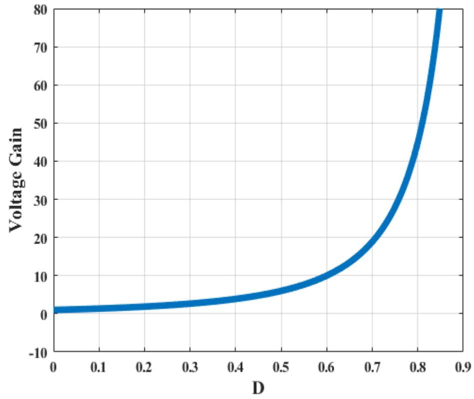


Fig4. The gain of the proposed converter in terms of duty cycle changes.

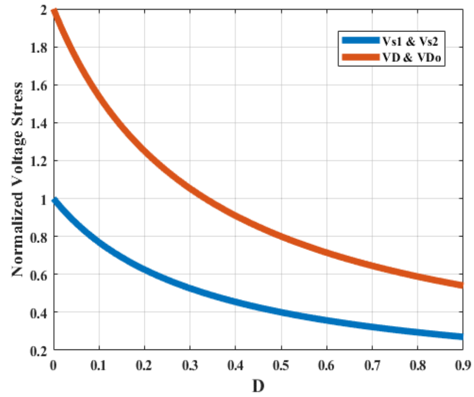


Fig5. Normalized stress of the converter's semiconductor elements.

3- Passive elements and proposed converter capacitors

In this part, the design relationships of passive elements such as inductors L_1, L_2, and L_3 and capacitors C_o and C are expressed. The basic inductor relationship is used to design the L_1 and L_2 inductors, which are equal, where D is the duty cycle, Δi_L is the inductor current ripple, and f is the switching frequency.

$$L_1 = L_2 = \frac{DV_{in}}{f\ \Delta i_L} \tag{10}$$

To calculate the size of L_3, it should be considered that the voltage across the inductor in the first state is equal to 2Vin. Therefore, the below equation is introduced to obtain the value of inductor L_3:

$$L_3 = \frac{2DV_{in}}{f\ \Delta i_{L3}} \quad (11)$$

The equivalent series resistance (ESR) is not considered when designing the output capacitor. The capacitance value is determined based on the output power, desired voltage ripple, and switching frequency of the converter.

$$C_O = \frac{D\, I_o}{f\ \Delta V_o} \quad (12)$$

Capacitors C_1 and C_2 can be considered equal. Since they supply the load current, according to the capacitor base relation, their values are determined as follows:

$$C_1 = C_2 = \frac{I_o}{f\ \Delta V_C} \quad (13)$$

1. Simulation results

The theoretical analysis of the proposed high step-up converter was verified through simulations using PSpice software. Figure 6 shows the schematic of the simulation circuit for the high step-up SEPIC converter. Table 1 presents the specifications of the elements used in the converter, designed for an input voltage of 40 V and an output voltage of 270 V with a switching frequency of 50 kHz.

The gate-source voltage of the switches is depicted in Figure 7, and Figure 8 illustrates the waveforms of drain-source voltage and current for switch S1. These waveforms show that the switch current increases with a slope during turn-on and turn-off, indicating a zero-current switching (ZCS) operation. Similarly, Figure 9 presents the drain-source voltage and current waveforms for switch S2, which exhibit similar ZCS behavior. The current waveforms for diodes D and Do are shown in Figures 10 and 11, respectively, revealing that the diodes operate with decreasing current slopes and turn off with no reverse recovery issue, indicating ZCS operation. This implies that all the semiconductor elements in the proposed high-voltage gain converter operate under soft-switching conditions, resulting in minimal conduction losses.

Table 1. Specifications of important elements of the proposed high-amplification converter.

Specification	Element	Icon
V 40	Input voltage	V_{in}
V 270	Output voltage	V_{out}
W 140	Output power	P_{out}
KHz 50	Switching frequency	f_{sw}
μF 10	Capacitors	C_1, C_2
μF 47	Output capacitor	C_o
IRF740	Main key	S_1-S_2
MUR860	Diodes circuit	D-D_o
0.6	Duty cycle	D

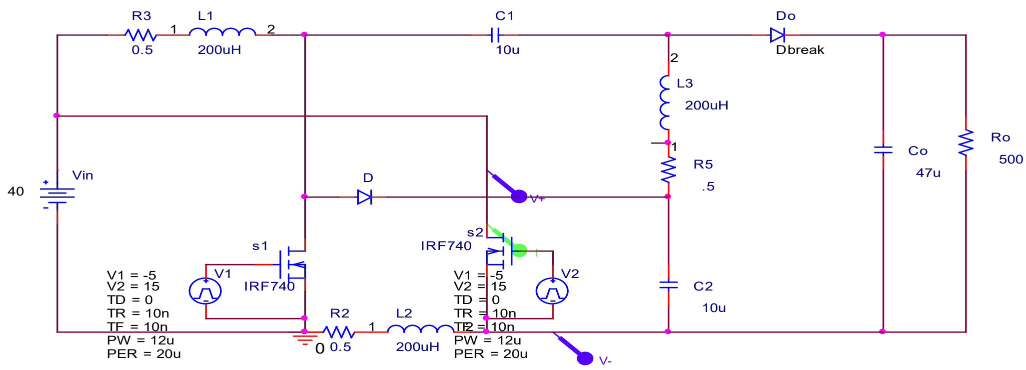


Fig.6. Schematic of the proposed high-gain SEPIC converter in PSpice software.

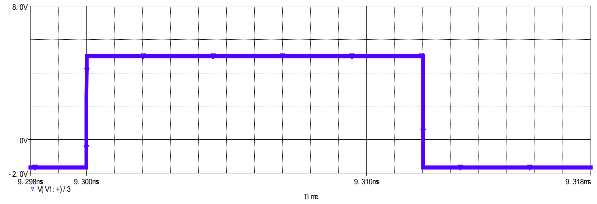


Fig.7. The gate-source voltage waves of switches (6V/div, 1µs/div).

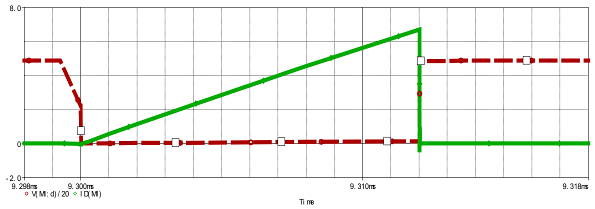


Fig.8. Drain-source voltage (red) and current (green) of switch S (2A/div, 40V/div, 1µs/div).

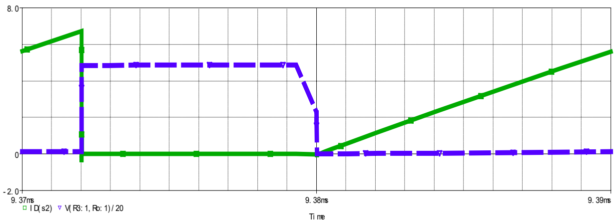


Fig.9. Drain-source voltage (red) and current (green) of switch S (2A/div, 40V/div, 1µs/div).

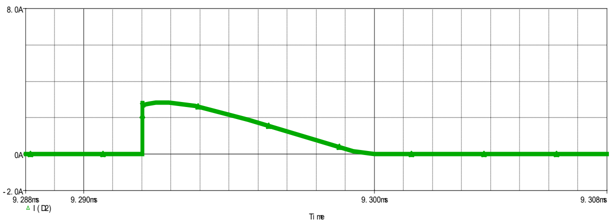


Fig.10. D diode current (2A/div, 1µs/div).

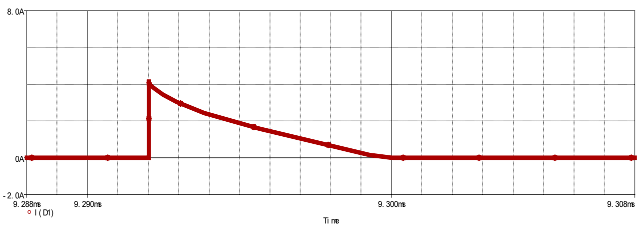


Fig.11. Do diode current (2A/DIV, 1µS/DIV).

5. Experimental results

In this section, a laboratory prototype of the proposed high step-up converter has been implemented to verify the correctness of the simulation results. Fig. 12 shows a photograph of the laboratory prototype of the converter. Switches and output diode waveforms are shown in Fig. 13. As can be seen, the following results confirm the presented simulation results.

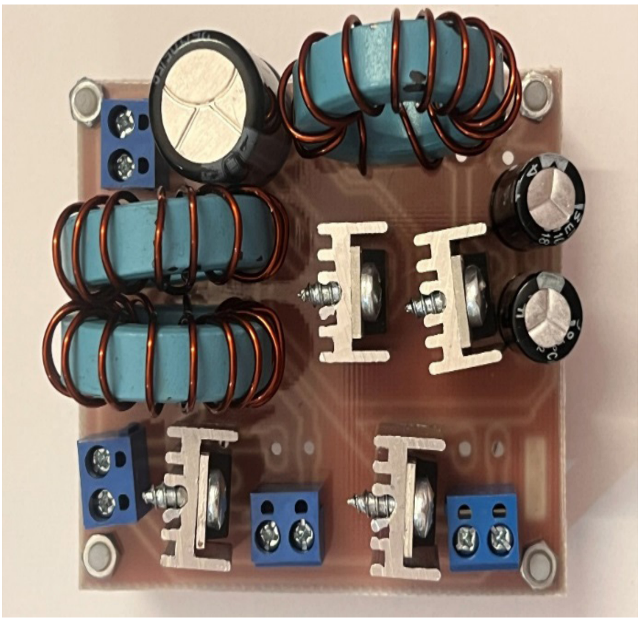
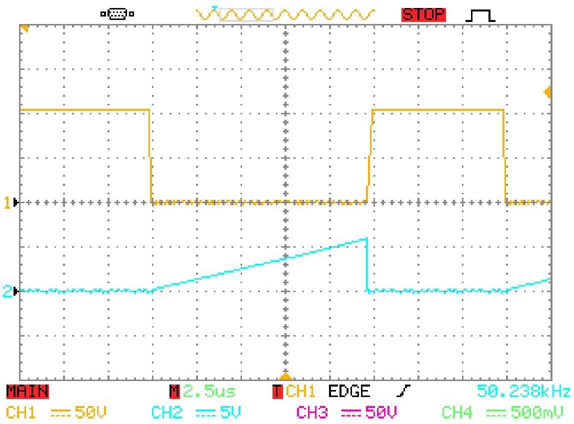
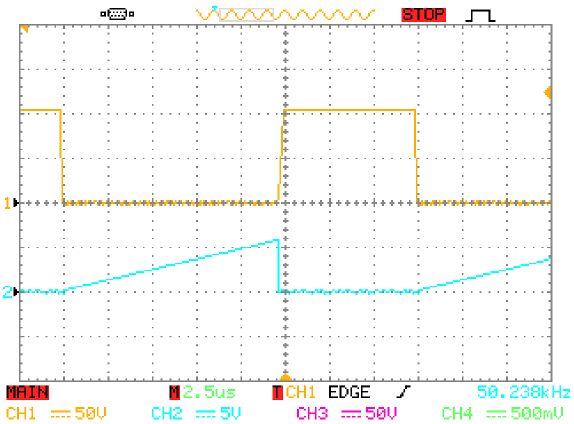


Fig.12. Schematic of the laboratory sample of the proposed converter.

(a) Voltage and current waveform of switch S1.



(b) voltage and current waveform of switch S2.



(c) Output diode current waveform.

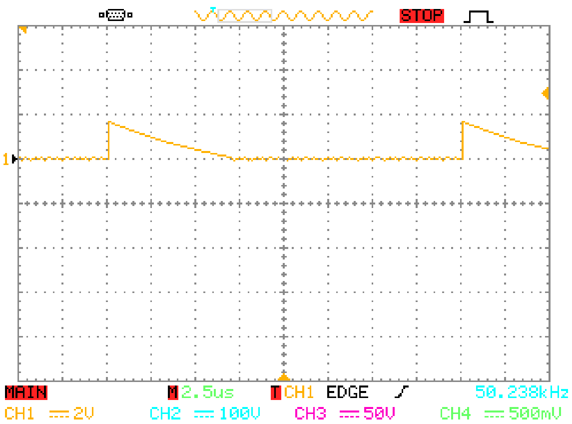


Fig.13. Waveforms of the laboratory sample of the proposed converter.

In the practical current waveform of the switches, the current increases with the slope, and as a result, the ZC condition is established. Also, the current of the output diode has decreased with a slope of zero, so the ZC conditions for its turning off are met, eliminating the diode reverse recovery problem.

6. Comparison of the proposed converter with similar converters

In this section, the proposed converter is compared with similar converters in Table. 2. As can be seen, the number of converter elements is higher than in [34], [35], and [38] converters, but the mentioned converters have a lower voltage gain than the proposed converter. On the other hand, the input current in the converters in [37] and [38] is pulse, which is unsuitable for photovoltaic applications. Also, the voltage stress of the proposed converter switch is less than that of the other converters, so it is possible to use more efficient switches with lower conductive resistance, and as a result, the conductive losses caused by the switches are reduced. Two switches are used in the proposed converter, but since they receive the same command pulse, the control circuit is not more complicated.

Table 2. A comparison between the accomplishment of the proposed converter and other converters in [34-38].

Converter	Voltage Gain	Voltage stress of Switches	Voltage stress of Diodes	No. of elements S D L C	Total Component Count	Input current
Proposed Converter	(1+3D)/(1-D)	Vo/(1+3D)	2Vo/(1+3D)	2 2 3 3	10	Continues
[34]	(1+D)/(1-D)	Vo/(1+D)	Vo/(1+D)	1 2 2 3	8	Continues
[35]	1/(1-D)	Vo	Vo	1 2 3 3	8	Continues
[36]	3D/(1-D)	Vo/3D	Vo/3D	1 3 4 6	14	Continues
[37]	-3D/(1-D)	Vo/3D	Vo/3D	1 3 3 5	12	Pulse
[38]	2D/(1-D)	Vo/2D	Vo/2D	1 2 2 3	8	Pulse

Conclusion

The growing utilization of renewable energy sources has led to increased demand for interface converters to increase output voltage levels. Soft-switching techniques, like zero-current-switching, are commonly employed in high step-up converters because they raise the switching frequency, reduce circuit size and weight, and minimize switching losses. This paper presents a high-voltage gain converter that addresses some of these issues. Noteworthy features of this switching converter include ZCS operation during switch turn-on, a low number of converter elements, the absence of the reverse recovery problem in diodes, and low switch voltage stress. Additionally, the proposed converter eliminates the need for coupled inductors and an additional switch, providing further advantages. Also, the voltage stress of the switch is lower than the output voltage, which leads to the use of switches with smaller R_{DS}(on) and subsequently reduces conduction losses. One limitation of the converter is that the input and output grounds are not common. Future research could focus on designing and implementing a control circuit for the converter, reducing conduction losses in the auxiliary circuit, and minimizing the number of capacitors and diodes in the auxiliary circuit to enhance overall performance.

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