HYDROGEN, FUEL CELL & ENERGY STORAGE

A new ZVT interleaved high step-up converter with ripple cancellation for photovoltaic systems

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Abstract

This study introduces a high step-up converter that utilizes a winding cross-coupled inductor paired with a novel auxiliary circuit. The auxiliary circuit facilitates zero-voltage switching (ZVS) for the main switches while ensuring zero-current switching (ZCS) for the auxiliary switch. Besides, a ripple cancellation technique is employed to reduce input current ripple. The converter achieves high voltage gain, thereby reducing voltage stress on the main switches. Moreover, the auxiliary switch operates for a brief period, keeping the circulating current in the auxiliary circuit low and minimizing associated losses. On the other hand, the auxiliary circuit has a low number of components and can be expanded to more parallel branches of the converter without increasing the number of switches. The proposed converter's design and functionality have been rigorously analyzed and verified through simulations using PSPICE software. Additionally, a 100 W prototype has been constructed to validate both the theoretical analysis and the simulation outcomes.

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1 Introduction

Photovoltaic (PV) panels in distributed solar power systems generally produce low voltage and high current. To mitigate this, a step-up DC-DC converter is utilized, as referenced in [1–3]. Traditionally, a boost converter is used for this purpose, but it encounters several major challenges in solar energy applications:

1. The switch is subjected to a voltage stress equal tothe output voltage.
2. Achieving a high step-up gain necessitates a high duty cycle, which increases conduction loss.
3. Reverse recovery problems in the diodes are caused by high voltage stress and elevated duty cycles.

Over the last twenty years, numerous high-gain DC-DC converter topologies have been developed to address these issues. These designs aim to minimize voltage stress and reduce the duty cycle of the switch, overcoming the limitations of the boost converters. Moreover, step-up converters support the efficient integration of small-scale clean energy sources such as solar panels and fuel cells into the grid [4–6].

References such as [4, 7, 8] explore high-gain power converters employing voltage doubler circuits or capacitor-diode cells. Despite achieving substantial voltage gain, these converters face efficiency challenges because of the voltage drop across diodes handling high currents. In [9, 10], converters with additional voltage gain utilizing multi-stage L-C-D cells have been proposed, which reduce switching stress but require many components. In [11], a high-voltage gain with high power converter is described, incorporating a dual active bridge (DAB) and transformer. However, its complex control requirements and extensive component needs may limit its suitability for standalone modular solar power systems. Meanwhile, [12] introduces a new non-isolated converter designed to integratephotovoltaic (PV) systems with a microgrid. It uses a Z-source converter with an interconnected inductor. This design achieves significant output voltage gain but also adds complexity and increases the number of components. To increase power levels, reduce input current ripple, and downsize magnetic components, step-up converters have adopted interleaving techniques. Conventional interleaved boost converters offer limited voltage gain, pleading to the development of coupled-inductors in interleaved structures for high voltage and high-power applications. The converter in [13] combines a voltage-doubler circuit with a flyback-boost topology to achieve substantial gain. The converters in [14, 15] integrate a traditional interleaved step-up circuit with a capacitor switched and a multiplier with coupled inductor. The converter in [16], with inputs in parallel and outputs in series, incorporates a confirmed two-phase converter with a voltage multiplier element to attain substantial voltage gain. In [17], a two phase converter combines a coupled inductor with two voltage-doubler circuits for high voltage conversion. A step-up converter utilizing ZVS with four switches, described in [18], incorporates a regenerative snubber that recycles leakage energy and enables the diodes to achieve zero-current switching (ZCS). References [19, 20] describe interleaved multiple- windings high-gain converters to reach adjustable voltage gain. In the converter described in [20], the current ripple is minimized while achieving a high voltage gain. However, the converter has four active switches, with two of them experiencing high stress on the output side. This not only imposes a high cost but also reduces its reliability.

The ZVS converters discussed in [21–26] employ magnetic techniques to enhance voltage gain. Converter [21] has a small number of components, but its main disadvantage is the voltage stress on the output diodes and their reverse recovery issue. The converter in [22] features a minimal number of components and provides a high voltage gain, but due to the hard switching of the elements, high switching losses are inevitable. Converter [23] has a simple structure with only two active switches, but it faces issues with hard switching and a pulsed input current, making it unsuitable for photovoltaic systems. The active clamp technique discussed in [24–26] involves a capacitor and an extra MOSFET, with each pair connected in parallel with a main MOSFET. The main problems of active clamp converters is the high circulating current in the auxiliary circuit and the loss of ZV conditions in light load.

In this paper, a new high voltage gain interleaved converter with minimal current ripple is presented. One of the key features of the converter is the small number of auxiliary circuit elements and its modularity. Additionally, switching the devices at zero voltage has eliminated the capacitive turn-on losses in the switches.

2 The Proposed step-up interleaved DC-DC converter

The proposed high step-up interleaved converter, shown in Figure 1, includes two main switches (M_1 and M_2), an auxiliary switch (M_a), auxiliary inductor (L_a), snubber capacitor (C_S), and coupled inductors (L_1-L_4 and L_2-L_3). The magnetizing inductors in the coupled inductors are labeled as L_{m1} and L_{m2}, while the

leakage inductors are designated as L_{K1} and L_{K2}. To decrease input current ripple, the coupling inductors are configured in parallel at the input and connected in series at the output. Diodes D_1 and D_2, along with capacitors C_1 and C_2, are incorporated to enhance the voltage gain. The converter also comprises an output diode (D_o) and an output capacitor (C_o). Additionally, the auxiliary circuit features auxiliary diodes (D_{a1} and D_{a2}).

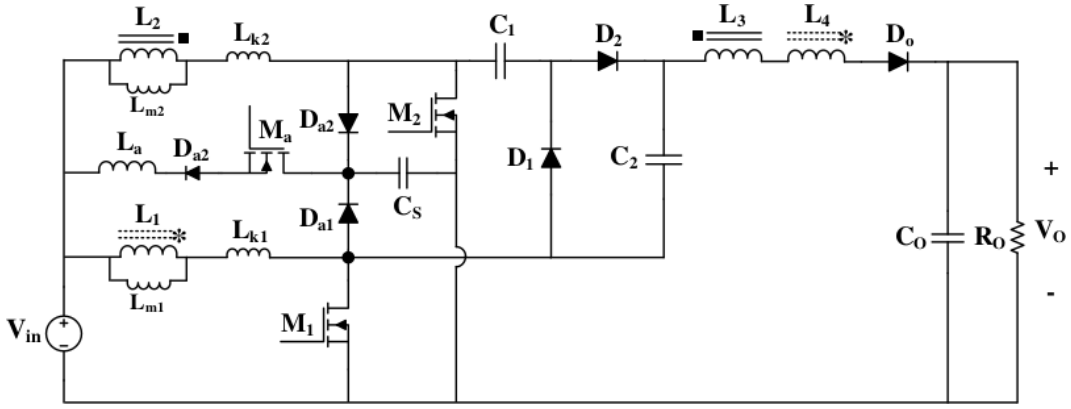


Fig. 1. Schematic view of the proposed high step-up interleaved converter.

2.1 Operation of the proposed converter

The proposed converter operates in eight different states within each cycle. The primary switches are controlled with a 180-degree phase shift. The auxiliary switch is activated slightly before the main switches and is turned off immediately afterward. For simplification in analysis, it is assumed that the magnetization current and the voltages across capacitors C_1, C_2, and C_o remain constant. Additionally, the components are considered ideal. Figure 2 illustrates the primary waveforms, while Figure 3 presents the corresponding equivalent circuit for each converter state.

First state This state begins with Ma being turned on. The inductor L_a enables M_a to turn on under Zero-Current (ZC) conditions. As capacitor C_S starts resonating with L_a, it discharges C_S, which then causes the anti-parallel diode of M_2 to conduct. Consequently, M_2 can now turn on under Zero Voltage (ZV) conditions.

Second state At the beginning of the mode, the current shifts from the body diode of M_2 to M_2 itself, causing the current to increase with a slope determined by inductor La until it reaches I_{Lm2}. As a result, both inductors L_{m1} and L_{m2} charge linearly. The La voltage across L_a reverses, and its current declines linearly. By the end of this state, M_a is turned off under ZC conditions.

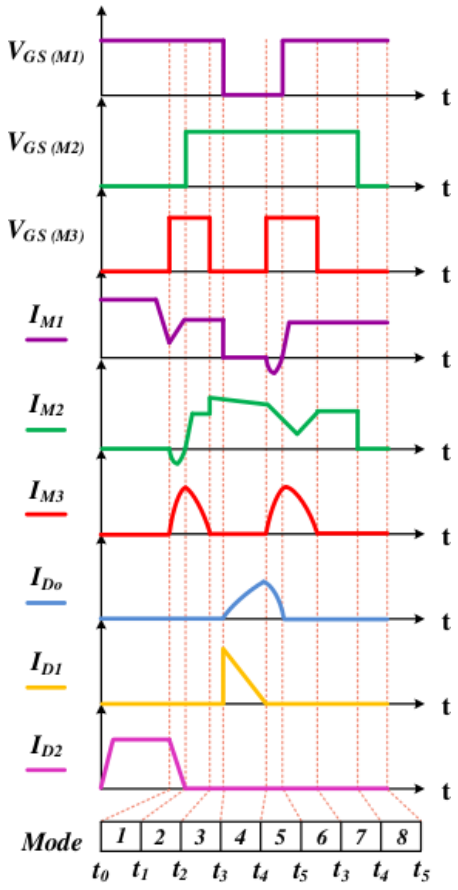


Fig. 2. Key waveforms of the introduced interleaved converter.

Third state In this state, the auxiliary switch is deactivated under ZC, disconnecting the auxiliary circuit from the converter. The output capacitor then provides power to the load.

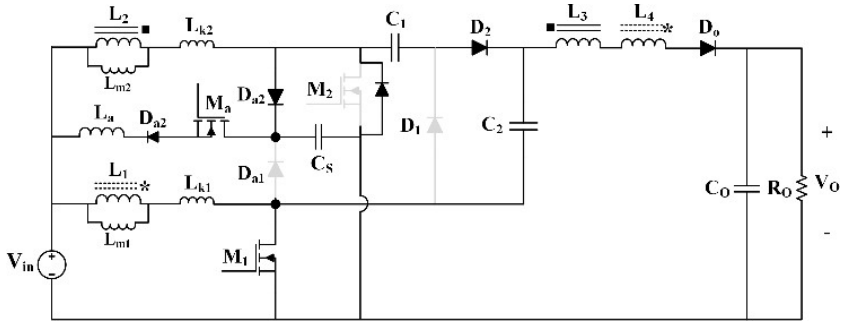
Fourth state Here, M_1 is turned off, and the energy from L_{k1} discharges through diode D1into capacitor C_1. Additionally, the energy from the magnetizing inductor is transferred to the output via the diode D_o.

Fifth state In this state, M_a is activated, , causing C_S to discharge. The body diode of M_1 conducts, allowing M_1 to turn on under ZV conditions.

Sixth state In this state, M_1 is turned on under ZV conditions, causing the output diode to turn off. Simultaneously, a reverse voltage is applied across L_a, causing it to discharge linearly. As the current through M_a decreases, the current through M_2 increases until it reaches I_{Lm2}. This state concludes when M_a is turned off under ZC conditions.

Seventh state In this state, M_a is turned off under ZC conditions, with both switches M1 and M2 remain on, allowing both magnetizing inductors to charge. The output capacitor continues to supply current to the load.

Eighth state In this state, switch M2 is deactivated, causing its voltage to rise linearly as the capacitor Cs charges, allowing M2 to turn off under ZV conditions. Meanwhile, M1 remains on, leading to the linear charging of Lm1. The output capacitor continues to supply current to the load.



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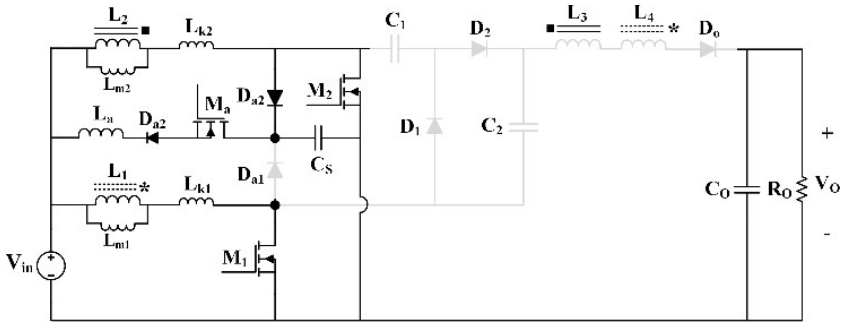

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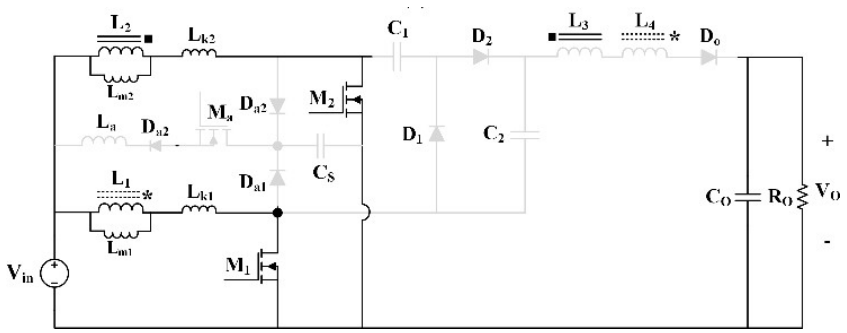

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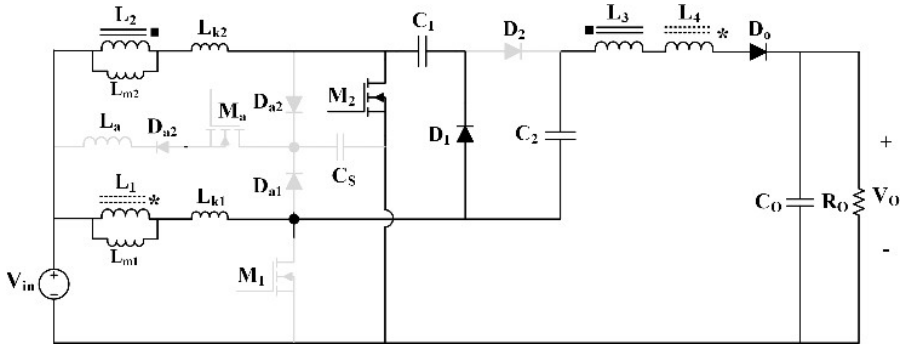
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L3
L4
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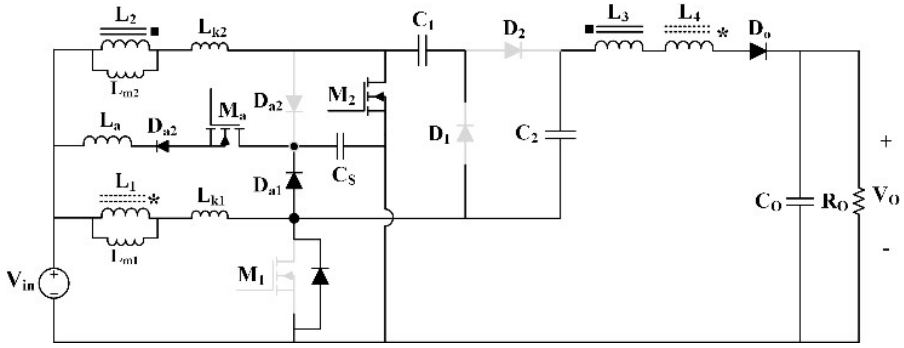
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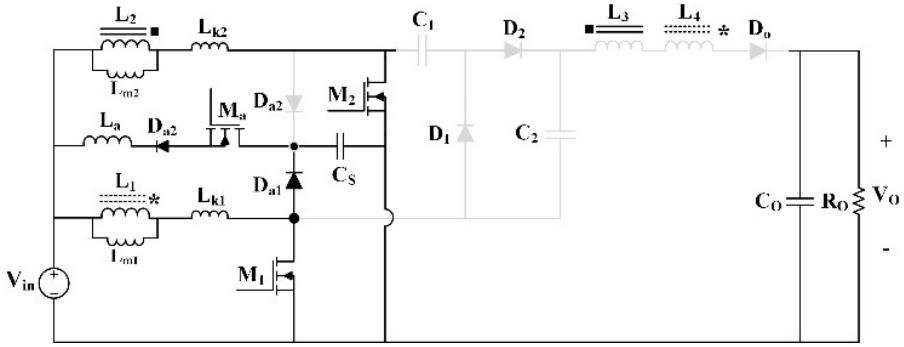
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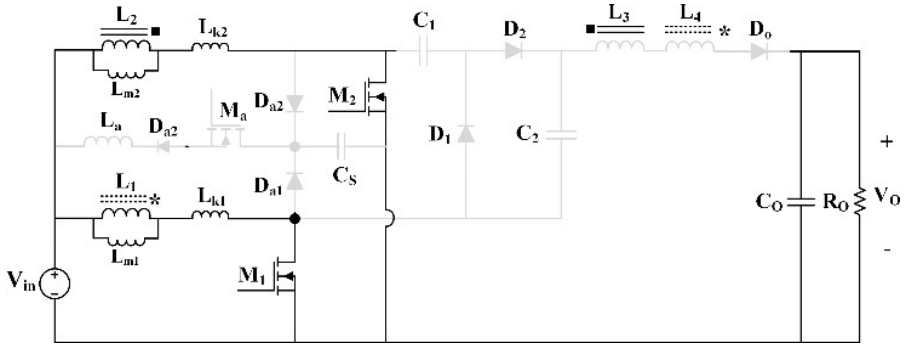
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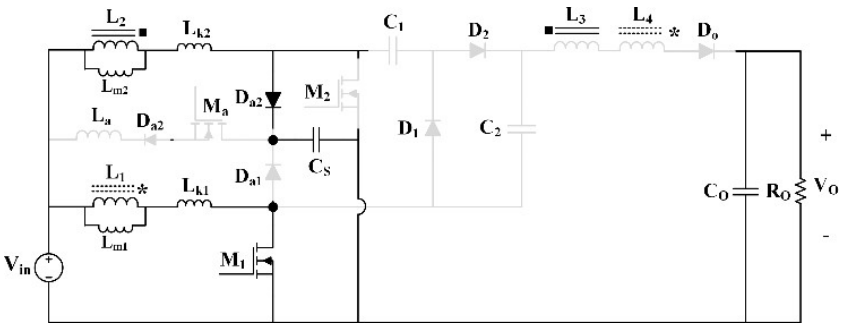


(h)

Fig. 3. The equivalent circuit of each state of the proposed converter.

3 Analysis of the proposed converter

This section investigates the analysis of the proposed converter, including calculations of gain, voltage stress, and other relevant parameters.

3.1 Voltage gain

Suppose $n = n_2/n_1$. Applying the volt-second balance to L_{m1} yields the following relationship

$$V_{C_1} = \frac{V_{in}}{1-D}\,. \tag{1}$$

Also, capacitor C_2 is charged twice as much as capacitor C_1.

$$V_{C_2} = \frac{2V_{in}}{1-D}\,. \tag{2}$$

Therefore, the voltage gain is calculated as follows.

$$\frac{V_o}{V_{in}} = \frac{3+n}{1-D}\,. \tag{3}$$

Figure 4 illustrates how the gain of the proposed converter varies with changes in both the duty cycle and the turn ratio.

The leakage inductance causes a decrease in the voltage drop across the primary, leading to changes in the following relationships:

$$k = \frac{L_m}{L_m + L_k} \tag{4}$$

$$V_{C_1} = k\,\frac{V_{in}}{1-D} \tag{5}$$

$$V_{C_2} = 2k\,\frac{V_{in}}{1-D} \tag{6}$$

$$\frac{V_o}{V_{in}} = k\,\frac{3+n}{1-D} \tag{7}$$

where k is coupling factor.

3.2 Voltage stress of elements

The voltage stress on the components can be easily calculated by applying Kirchhoff's Voltage Law (KVL) as follows:

$$V_{M_1} = V_{M_2} = \frac{V_{in}}{1-D} = \frac{V_o}{3+n}\,, \tag{8}$$

$$V_{D_1} = V_{D_2} = \frac{2V_{in}}{1-D} = \frac{2V_o}{3+n}\,, \tag{9}$$

$$V_{D_o} = V_o + \frac{n-2}{1-D}V_{in} = \frac{1+2n}{3+n}V_o\,. \tag{10}$$

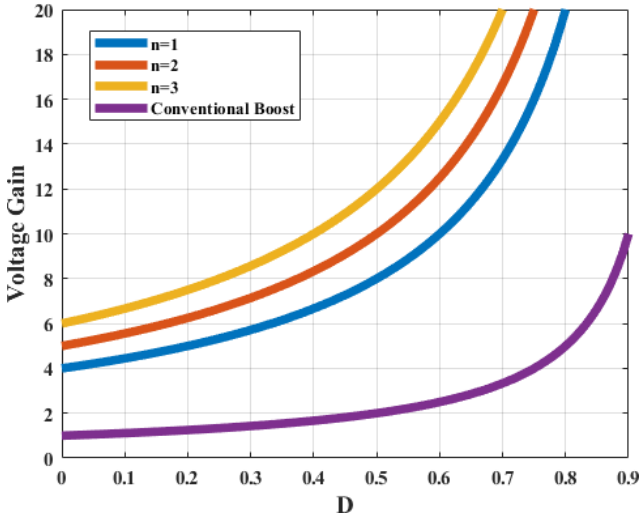


Fig. 4. The graph of the converter's gain as it varies with changes in both the duty cycle and turn ratio compared to boost converter gain.

Figure 5 illustrates the normalized stress on switches S_1 and S_2, as well as on diodes D_1, D_2, D_o.

3.3 Output capacitor design

The output capacitor supplies current for a duration of $(2D-1)T$. Therefore, the size of C_o can be determined as follows:

$$i_c = C\frac{dv}{dt} \tag{11}$$

$$C_o = \frac{I_o(2D-1)}{\Delta V_o f} \tag{12}$$

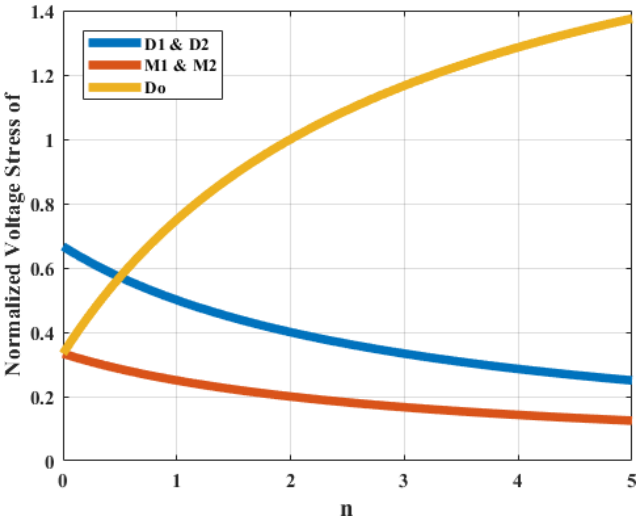


Fig. 5. The diagram of the normalized stress of the semiconductors components.

4 Simulation and practical results of the proposed high step-up interleaved converter

To verify the analysis of the proposed converter, simulations were performed using PSPICE software with an output voltage of 420 V, an input voltage of 24 V, and a power rating of 240 W. Table 1 presents the specifications of the designed components. Furthermore, Figure 6 depicts the schematic of the introduced interleaved high-gain converter within the software, while Figures 7-12 showcase the simulation results. Figures 7 and 8 illustrate the current and voltage waveforms of the main switches M_1 and M_2. As shown in these figures, the current through the switches is negative when they are turned on, causing the anti-parallel diode to conduct and ensuring that the switching conditions are established at zero voltage for the switches. Thus, there are no capacitive turn-on losses. Meanwhile, the voltage across the switches increases with a slope during turn-off, due to the presence of the snubber capacitor, indicating that the main switches turn off under zero-voltage (ZV) conditions. Figure 9 displays the current and voltage waveforms of Ma, showing that the current rises and falls in a manner consistent with zero-current (ZC) conditions for both the on and off states of the auxiliary switch. Figure 10 presents the current waveform for the output diode D_o, demonstrating that ZC conditions are met for the output diode. Figure 11 shows the current waveforms for diodes D_{a1} and D_{a2}, as well as for the diodes in the auxiliary circuit, indicating that these diodes also turn on and off under ZC conditions without issues related to reverse recovery. Similarly, Figure 12 displays the current waveforms for diodes D_1 and D_2, confirming that these diodes also turn off under ZC conditions and do not experience reverse recovery problems. Therefore, the converter diodes do not contribute to substantial conduction losses. The only issue is the capacitive turn-on losses in the auxiliary switch. To reduce these losses, the turn ratio of the third winding should be increased. Finally, Figure 13 shows the image of the implemented converter, which is built with a power rating of 220 W to validate the simulation results. Figure 14 illustrates the voltage and current of the switches, as well as the current through the circuit diodes, verifying the simulation results. Figure 14d shows the input current ripple, indicating a low ripple current compared to the pulsed input current.

Table 1. Details of the proposed converter and the values of its elements.

Specifications/Elements	Component name/Value
All switches	IRF740
All diodes	MUR860
L_1, L_2	200 μH
Turns ratio=N	1
L_a	4 μH
C_s	10 μF
P_O	100 W
f_S	50 kHz
C_1 - C_2	10 μF
C_o	10 μF

5 Contrasting the efficiency of the suggested converter with its hard-switching counterpart

Figure 15 compares the efficiency of the proposed converter compared to a hard-switching variant (without an auxiliary circuit). he proposed converter demonstrates a 7% improvement in efficiency at full load. Notably, the efficiency of the proposed converter remains relatively stable as power decreases, while the hard-switching converter experiences a significant efficiency drop. This decline in the hard-switching converter is attributed to the passive clamp circuit, which introduces additional resistance and switching losses in the switches.

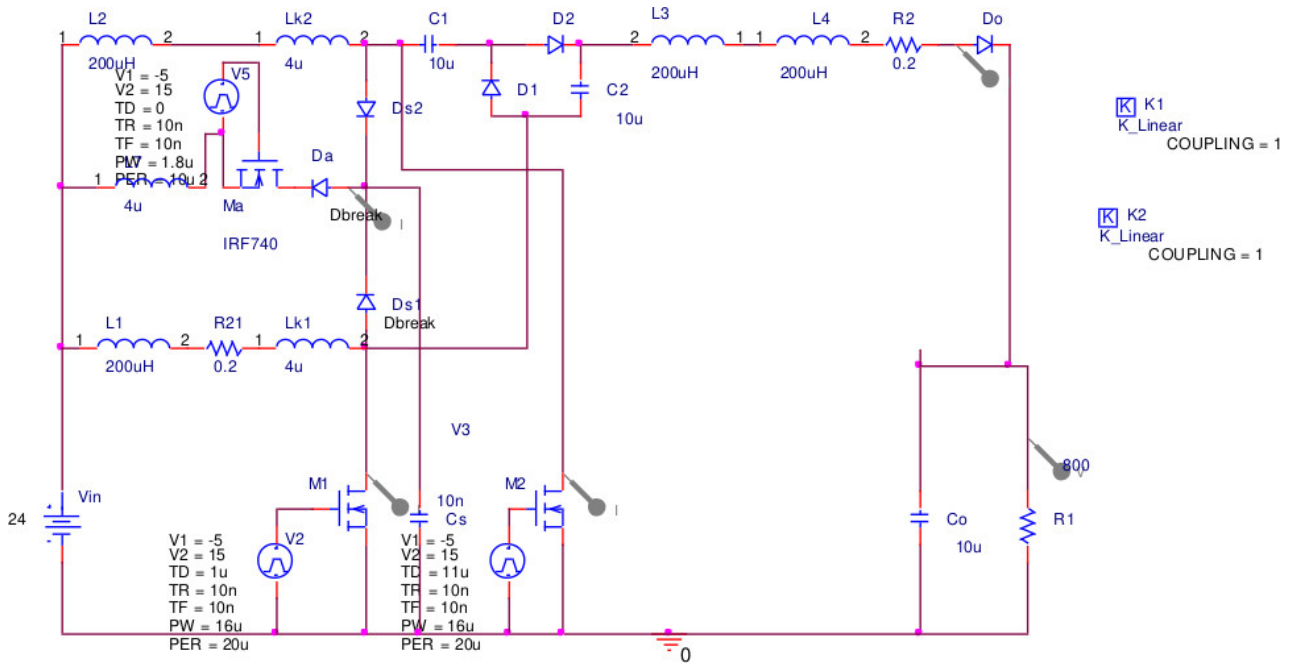


Fig. 6. Schematic of the simulated converter of the suggested interleaved high-voltage converter in PSPICE software.

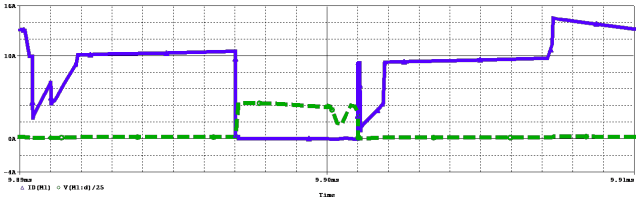


Fig. 7. The waveform of current (blue) and voltage (green dashed) of switch M_1 of simulated converter in scale of (2 μs/div, 2 A/div, 50 V/div).

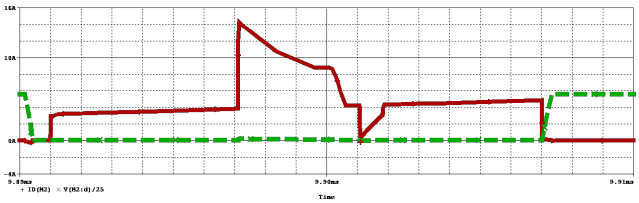


Fig. 8. The waveform of current (red) and voltage (green dashed) of switch M_2 of simulated converter in scale of (2 μs/div, 2 A/div, 50 V/div).

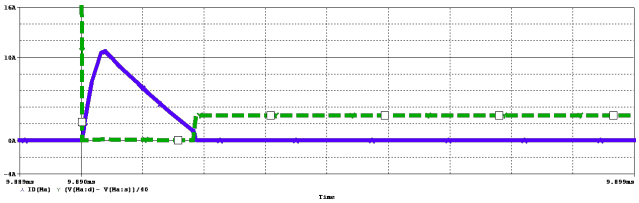


Fig. 9. The current (blue) and voltage (green dashed) waveforms of the switch M_a of simulated converter in scale (2 μs/div, 2 A/div, 80 V/div).

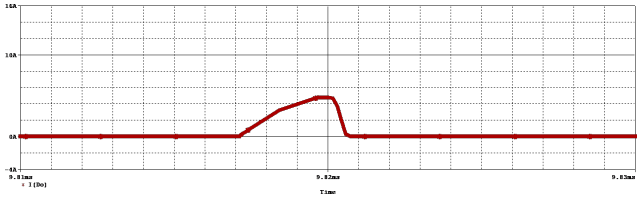


Fig. 10. The simulated current of the D_o in scale of (2 μs/div, 2 A/div).

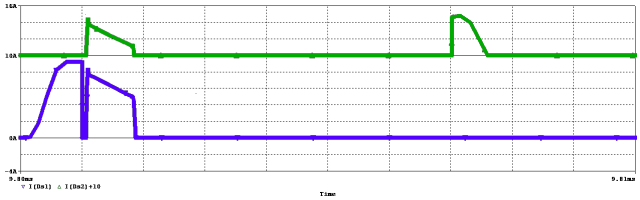


Fig. 11. The current waveform of auxiliary diodes D_{a1} (bottom) and D_{a2} (top) of the simulated converter in scale of (1 μs/div, 2 A/div).

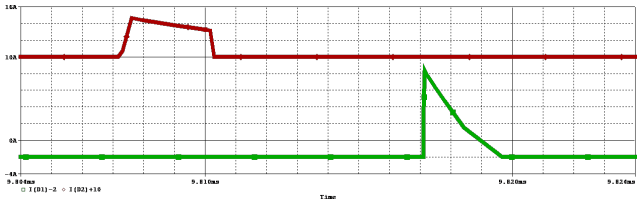


Fig. 12. The current waveform of diodes D_1 (bottom) and D_2 (top)of the simulated converter in scale of (2 μs/div, 2 A/div).

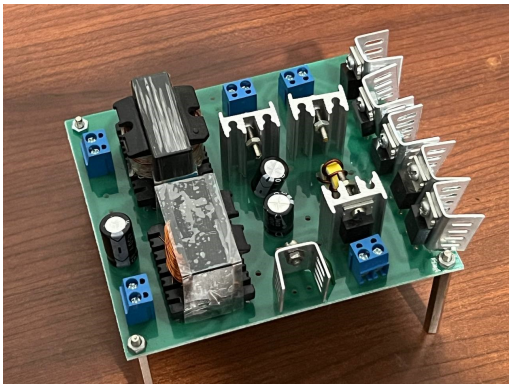
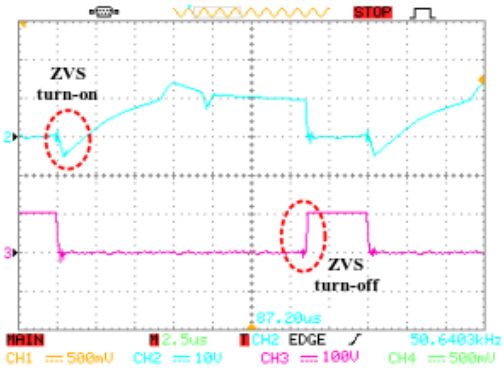


Fig. 13. The photograph of the proposed converter.



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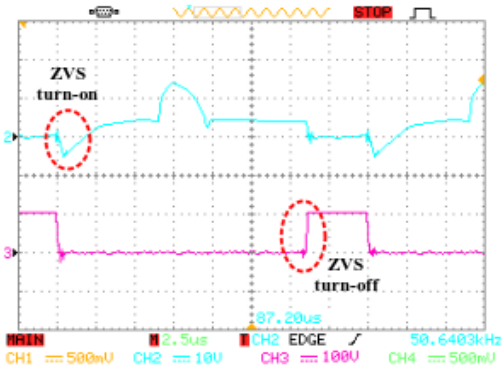

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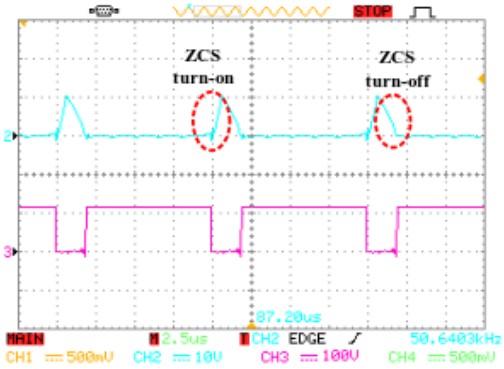

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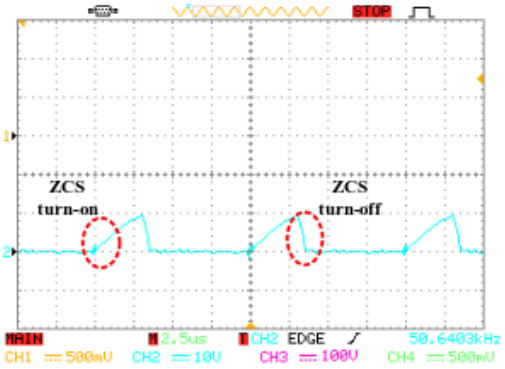

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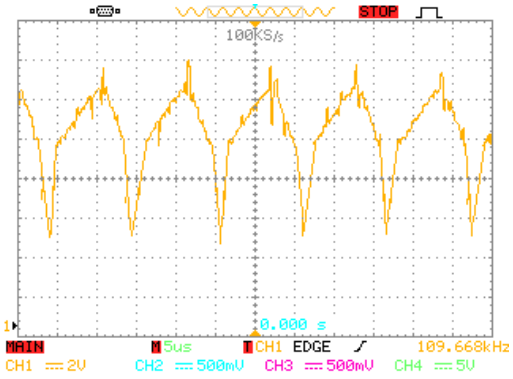

(e)

Fig. 14. The experimental waveforms of the proposed interleaved converter (a) Current (top) and voltage (bottom) of M_1 (b) Current (top) and voltage (bottom) of M_2 (c) Current (top) and voltage (bottom) of M_a (d) Current of D_o (10 A/div, 100 V/div, 1 μs/div) (e) Input current of the converter (2 A/div, 5 μs/div).

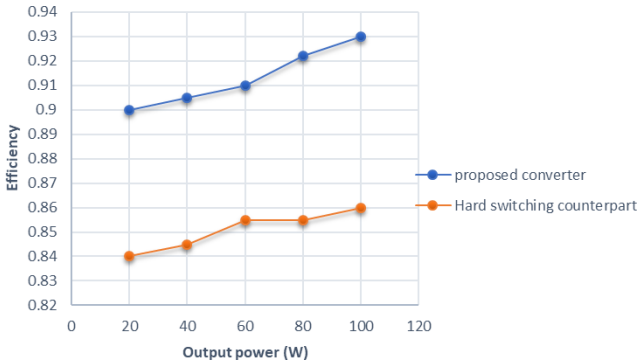

Fig. 15. The efficiency chart of the proposed converter compared to the hard-switched counterpart.

Table 2. The comparison of the operational performance of the proposed converter with similar ones.

Converter	Voltage gain	Stress of main switch	Number of components					Soft Switching
			Switch	Diode	Capacitor	Core	Total	
[21]	$\frac{2n+1-2nD}{1-D}$	$\frac{V_o}{2n+1-2nD}$	2	4	3	2	11	Hard
[22]	$\frac{n+nD+2}{1-D}$	$\frac{V_o}{n+nD+1}$	4	4	5	2	15	ZVS
[23]	$\frac{n+1}{1-D}$	$\frac{V_o}{n+1}$	4	4	3	4	15	ZVS
[24]	$\frac{2n+2}{1-D}$	$\frac{V_o}{2n+2}$	4	2	3	2	11	ZVS
[25]	$\frac{3n+1}{1-D}$	$\frac{V_o}{3n+1}$	3	10	6	3	19	ZVS
proposed	$\frac{n+3}{1-D}$	$\frac{V_o}{n+3}$	3	6	4	2	15	ZVS

6 Comparison of the converter performance

The proposed converter is evaluated against previous interleaved converters based on criteria such as voltage gain, stress on the main switch, type of switching, and the number of components, as summarized in Table 2. As shown, the proposed converter uses three switches, which is fewer than the converters in [22–24], each of which employs four switches in their design. Therefore, the proposed converter has a simpler control circuit and is more cost-effective to manufacture. The converter described in [21] has a minimal component count with only two switches, but its main drawback is hard switching, which leads to significant switching losses. The converter in [25] has the same number of switches as the proposed converter and offers high voltage gain. However, it includes a significantly large number of components and windings, resulting in noticeable conduction losses.

7 Conclusion

In this study, we introduced a high step-up ZVT interleaved converter designed with zero-voltage switching for the main switches, zero current switching for the auxiliary switch. The converter features minimal input current ripple, a streamlined auxiliary circuit, diodes with no reverse recovery issues, and low voltage stress on the main switches. Due to these features, the proposed converter is highly suitable for photovoltaic applications. It utilizes PWM control and supports the expansion of the auxiliary circuit to additional parallel branches without needing extra switches, while maintaining low circulating current in the auxiliary circuit. However, a primary drawback is the floating auxiliary switch source, which complicates its drive.

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