HYDROGEN, FUEL CELL & ENERGY STORAGE

An Improved Zero Current Transition High Step-Up Single-Switch Converter for Fuel Cell Applications

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Abstract

In this sudy, a new high step-up converter with reduced input current ripple and low voltage stress is presented. The converter features a minimal number of components, leading to reduced volume and cost. A lossless snubber is employed to achieve zero-current switching (ZCS) during turn-on and zero-voltage switching (ZVS) during turn-off. Additionally, all diodes operate under zero-current conditions, effectively eliminating reverse recovery issues. Furthermore, the snubber capacitor's stored energy is efficiently delivered to the output rather than being dissipated in the converter. Another advantage is that the energy from leakage inductances is captured by the lift capacitor, effectively eliminating voltage spikes on the switch. The proposed converter exhibits minimal input current ripple and outstanding efficiency, making it an excellent choice for integration into fuel cell systems. A comprehensive analysis of the converter has been conducted, and a 100W prototype has been both simulated and built to validate the circuit analysis. Experimental results demonstrate an efficiency of 95% under nominal load conditions.

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1 Introduction

Amid global energy shortages and growing environmental advocacy, distributed energy sources have gained significant traction worldwide. Among these, fuel-cell systems are particularly attractive due to their higher efficiency compared to traditional internal combustion engines and their ability to provide more reliable energy than other renewable sources. A fuel cell system is made up of fuel cell stacks, batteries, a high-gain DC-DC converter, and an inverter. A high voltage gain DC-DC converter is required to convert the low voltage of the fuel cell stacks (typically between 22 and 48 V) into an suitable DC link. This higher voltage is essential for powering standalone loads or transferring energy to the associated grid [1–3].

To efficiently achieve high voltage conversion, various improved high-gain converters have been developed. While traditional boost converters are among the simplest options, they suffer from practical limitations, including latch-up issues and a significant drop in overall efficiency as the duty cycle approaches unity. Additionally, these converters impose significant voltage stress on the switches, making low-voltage, high-performance devices unsuitable for such applications. Extreme duty cycles also result in large current ripples, increased conduction losses, and aggravated issues related to diode reverse recovery [4,5]. To enhance voltage gain, coupled-inductor and switched-capacitor techniques have been incorporated. However, in the converter presented in [6], all semiconductor devices operate under hard switching conditions, and the parasitic inductance of the coupled inductor generates voltage surges on the switch, leading to increased electromagnetic interference (EMI). These challenges can be mitigated by integrating clamp and snubber circuits, as proposed in [7]. Additionally, in [8], a converter is introduced that achieves an extremely high voltage conversion ratio by combining a multiplier cell with a voltage doubler.

Studies [9–11] explore high voltage conversion ratio techniques, achieving significant voltage gain and stable input current, thereby enhancing overall performance. However, switching losses affect their efficiency. Notably, the converter design presented in [12] stands out for its relative simplicity. The circuit topologies in [13] and [14] are quadratic converters that offer benefits such as ongoing input current, elevated gain, and reduced stress on the switch. In spite of these benefits, these converters operate under hard switching conditions, resulting in relatively low efficiency. To minimize switching losses, the most effective approach involves implementing soft switching techniques, including passive lossless snubbers [15, 16], active clamp circuits [17–19], and zero voltage transition (ZVT) methods [20–22].

The remainder of this study is organized as detailed below: Section 2 introduces the proposed circuit, detailing its structure and functional principles. Section 3 focuses on steady-state analysis and offers design guidelines. In section 4, simulations and experiments are presented. Section 5 compares the efficiency of the proposed converter with that of the same converter without the auxiliary circuit. Finally, section 6 compares the suggested step-up converter with previous similar designs.

2 Description of Proposed Converter

The proposed converter is demonstrated in Figure 1. It consists of an input inductor L_1, a pair of coupled inductors L_2-L_3, three large capacitors C_1, C_2 and C_3, an output capacitor C_o and three diodes D_o, D_1 and D_2. The auxiliary circuit includes a coupled-inductor L_{r1} and L_{r2}, an auxiliary D_a, and a snubber capacitor C_s. The main coupled-inductor is characterized by magnetizing inductance L_m and leakage inductance L_K in the model.

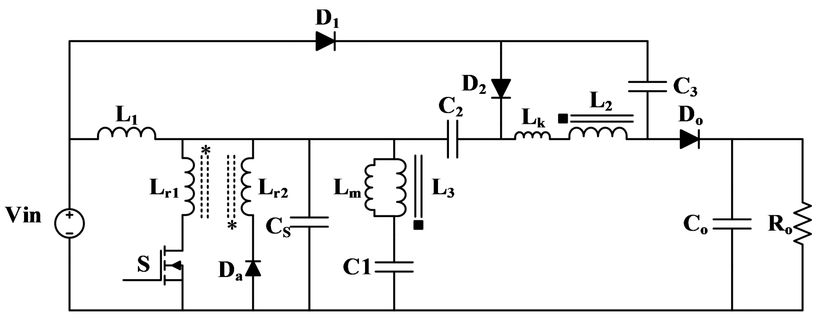


Fig. 1. Schematic representation of the proposed step-up converter.

2.1 The proposed converter operation

The converter operates in five distinct modes. Its switching waveforms are given in Figure 2 and the corresponding circuit configurations for each mode are illustrated in Figures 3 to 9. The voltage of capacitors C_1, C_2, C_3 and C_o remain constant during one cycle while the current of inductors L_1 and L_m also remain constant in one cycle due to its large value. Prior to the first interval, S is off and D_o and D_2 are on, and L_m energy is discharged through D_o at the output.

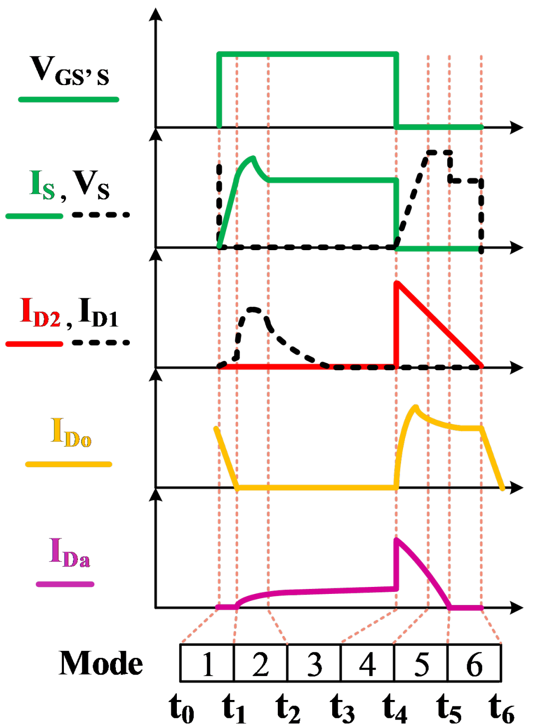


Fig. 2. Switching waveforms of introduced step-up converter.

The first mode: This mode starts when switch S is turned on. Since diode D_o is still on, the constant voltage across L_{r1} drops and the switch The current rises steadily from zero (ZC conditions). Meanwhile, the current through the output diode decreases linearly.

The second mode: This mode begins when D_o is turned off under ZC conditions. The resonant switch current increases until the resonant capacitor C_S is fully discharged through L_{r1} in resonance.

The third mode: In this mode, diode D_1 is turned on and capacitor C_2 is charged. The switch current is constant and inductor L_1 is charged linearly with a slope of V_{in}/L_1 . This interval ends when switch S is turned off.

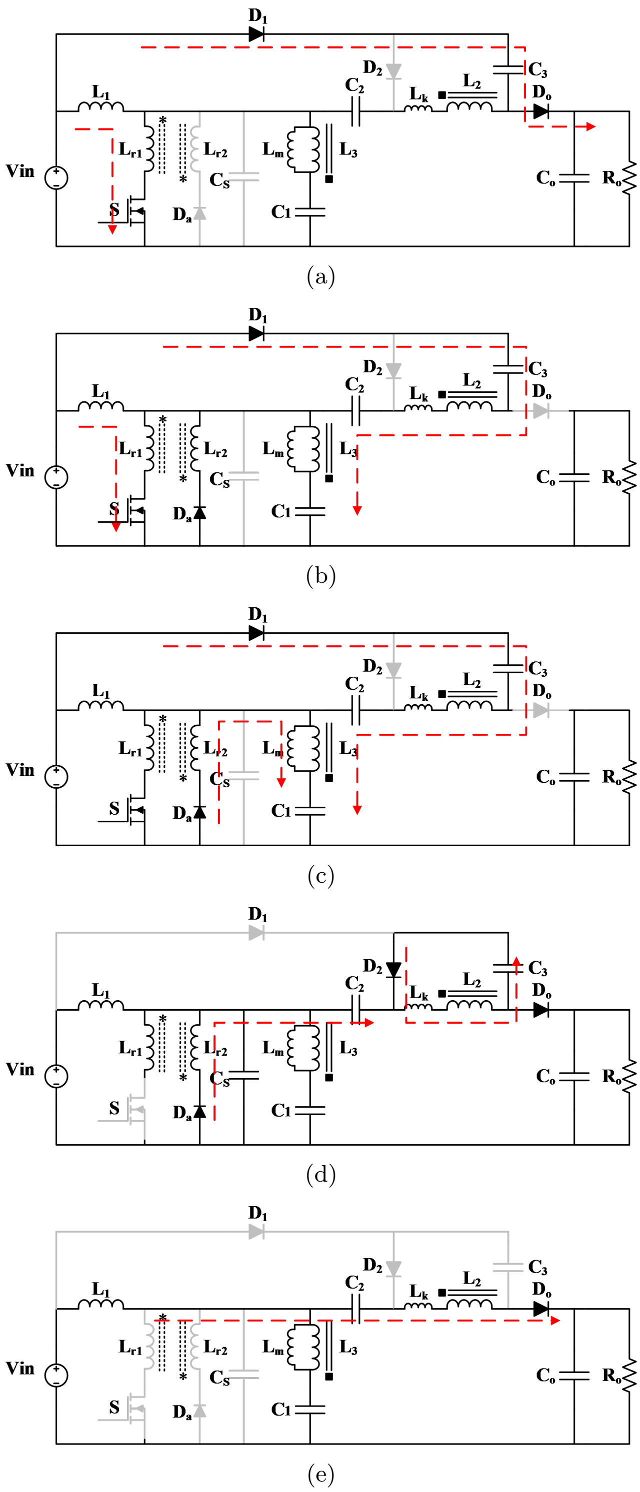


Fig. 3. Equivalent circuit of the proposed converter at the (a) first (b) second (c) third (d) fourth (e) fifth modes.

The fourth mode: This mode begins when switch S is turned off and inductor L_1 charges the snubber capacitor. On the other hand, diodes D_2, D_a and D_o are also turned on. Diode D_2 for charging C_3 and diode D_a for discharging L_{r1} in C_s and diode D_o for discharging L_m at the output provide the path.

The fifth mode: When L_{r1} and L_{r2} are fully discharged, diode D_a is turned off and auxiliary circuit is completely removed. Diodes D_2 and D_o are still on.

3 Evaluation of the Suggested Converter

3.1 Design of converter elements

According to the equation $\Delta Q = C\Delta V$, The equations for capacitor C_1, C_2 and C_o are easily calculated and expressed.

$$C_1 = \frac{I_o(1-D)}{\Delta V_{C_1} f}\,, \tag{1}$$

$$C_2 = \frac{I_o D}{\Delta V_{C_2} f}\,, \tag{2}$$

$$C_o = \frac{I_o D}{\Delta V_o f}\,. \tag{3}$$

By using the equation between the inductors, the inductors values will also be designed.

$$L_1 = \frac{V_{\text{in}} D}{\Delta I_{L_1} f}\,. \tag{4}$$

3.2 Design of L_{r1} and C_S

According to the design of snubber elements, L_{r1} and C_S will be calculated according to the following equations.

$$L_{r1} = \frac{V_{\text{SW}} t_r}{I_{\text{SW}}}\,, \tag{5}$$

$$L_{r2} = m^2 L_{r1}\,, \tag{6}$$

$$C_S = \frac{I_{\text{SW}} t_f}{V_{\text{SW}}}\,. \tag{7}$$

I_{SW} represents the current through the switch before it turns off, and V_{SW} denotes the voltage across the switch after it turns off, and t_r is the time taken for the switch current to rise, while t_f is the time taken for it to fall. m is also auxiliary coupled inductors turns ratio.

3.3 The proposed converter voltage gain

To compute the converter gain, it is enough to derive volt-second balance equation for L_1 and L_m. Figure 4 demonstrates the converter gain for different values of n and D.

$$V_{\text{in}} DT - \frac{V_o - (n+2)V_{\text{in}}}{2n+1}(1-D)T = 0\,, \tag{8}$$

$$V_{C_1} = (n+1)V_{\text{in}} + V_{C_2}\,, \tag{9}$$

$$V_{C_2} = n\frac{V_o - (n+2)V_{\text{in}}}{2n+1}\,, \tag{10}$$

$$M = \frac{V_o}{V_{\text{in}}} = \frac{D(n-1)+n+2}{}.1 - D \tag{11}$$

Figure 5 illustrates comparing the voltage gain of the introduced converter with different turn ratios against that of a traditional Boost converter.

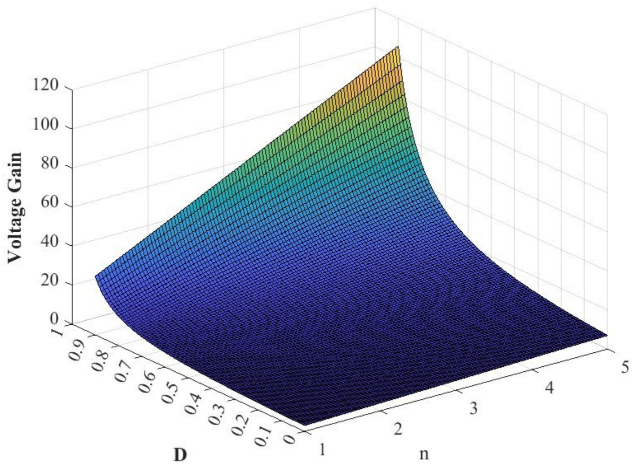


Fig. 4. The converter's gain for varying values of n and D.

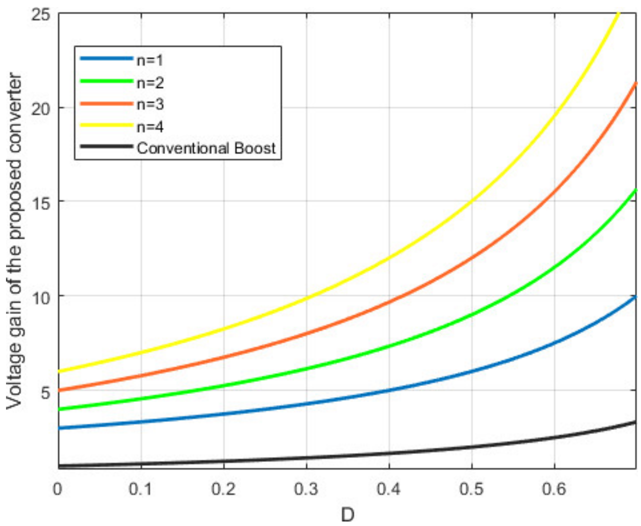


Fig. 5. Converter voltage gain compared to traditional Boost converter.

Considering the leakage inductance, the converter gain slightly decreases. In fact, the voltage drop across the leakage inductance leads to a reduction of the voltage gain. When accounting for the coupling factor, the converter gain can be calculated using the following equation. Figure 6 illustrates the gain of the proposed converter for a turn ratio of 2 and different coupling factors.

$$M_k = \frac{V_o}{V_{\text{in}}} = \frac{D(nk-1)+nk+2}{1-D}\,, \qquad (12)$$

where k is coupling factor.

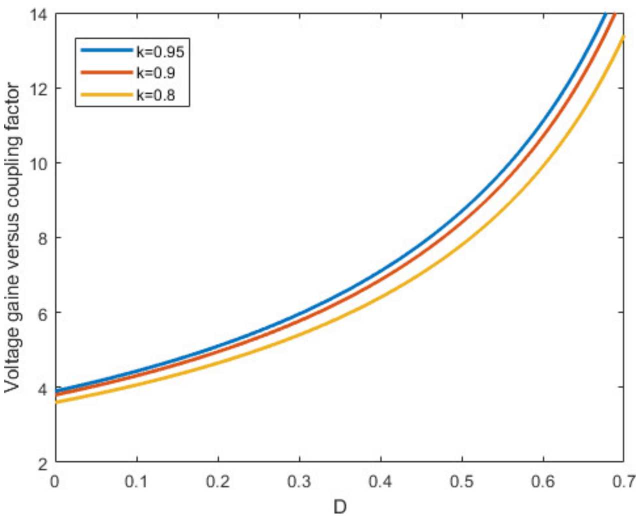


Fig. 6. The voltage gain versus coupling factor.

3.4 Voltage stress of elements

In CCM mode, voltage stress of diodes and converter switch will be as follows.

$$V_{D_o} = V_{D_1} = \frac{2n^2+3n+1}{(1+2n)(D(n-1)+n+2)} V_o\,, \qquad (13)$$

$$V_{D_2} = \frac{n}{D(n-1)+n+2} V_o\,, \qquad (14)$$

$$V_S = \frac{V_o}{D(n-1)+n+2)}\,. \qquad (15)$$

Figure 7 demonstrates the normalized voltage stress diagram of semiconductor devices with respect to output voltage for different values of n and duty cycle of 0.6.

3.5 Current stress of switch

Due to the presence of a series inductor with the switch in the snubber circuit and its resonance with the auxiliary capacitor during the second operating state, the switch current increases. This results in an increase in the switch current stress, as expressed in Equation (16). According to the equation, this stress has an inverse relationship with the impedance of the resonant tank and the turn ratio. However, with an optimized design, its impact will be negligible.

$$I_{\text{SW}}(\max) = I_{L_1} + \frac{V_o}{[D(n-1)+n+2]Z_r}\,, \qquad (16)$$

$$Z_r = \sqrt{\frac{L_{r1}}{C_s}}\,, \qquad (17)$$

where Z_r is impedance of the resonant tank.

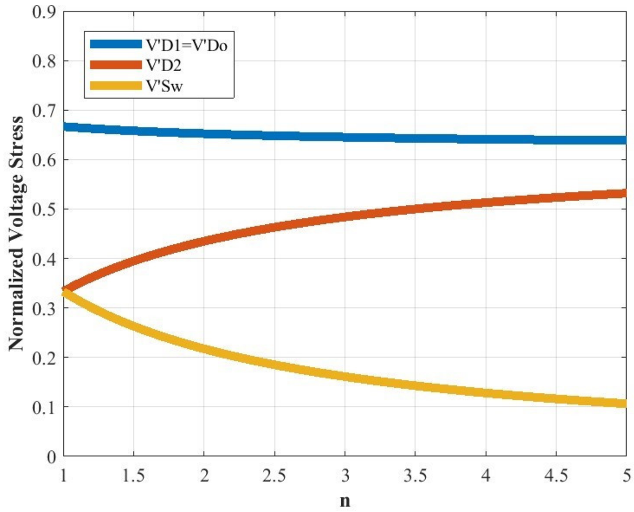


Fig. 7. Normalized voltage stress diagram of semiconductor devices with respect to output voltage for different values of n.

4 Simulation and Practical Results of Proposed Step-Up Converter

In line with the introduced converter analysis in the previous section, the converter elements are designed and simulated for a 100W power. The simulated circuit in PSpice software is demonstrated in Figure 8. The calculated values for converter parameters are provided in Table 1. Figure 9 shows the simulation waveforms of the switch voltage and current for the proposed converter. As it is clear, turning on the switch results in an increase in the current with a slope. The switchis turned on in ZC mode and at the moment it is turned off, the voltage rises with a slope, indicating that ZV conditions are provided for the switch to be turned off. Figure 10 illustrates the currents of diodes D_1 and D_2. As the current through one diode increases, the current through the other diode decreases, creating the ZC conditions. Consequently, both diodes are turned off in ZC mode, eliminating reverse recovery concerns. Figure 11 also demonstrates the current waveform of diodes D_o

and D_a, which shows that they are turned off in ZC mode. As a result, the circuit diodes are free from reverse recovery issues. Figure 12 presents the simulated waveforms of the input current of the proposed converter, highlighting its low ripple characteristics.

Figure 13 demonstrates the implemented circuit, while Figure 14 presents the current and voltage waveforms of the switch and diodes D_1, D_2, D_o, and D_a. As seen, As seen, the practical results confirm the simulation results and analysis conducted. ZC conditions for switching on the switch and ZV conditions for switching it off are identified by the slope of current and voltage. The currents of all the diodes also decrease with a slope, causing them to turn off in ZC mode.

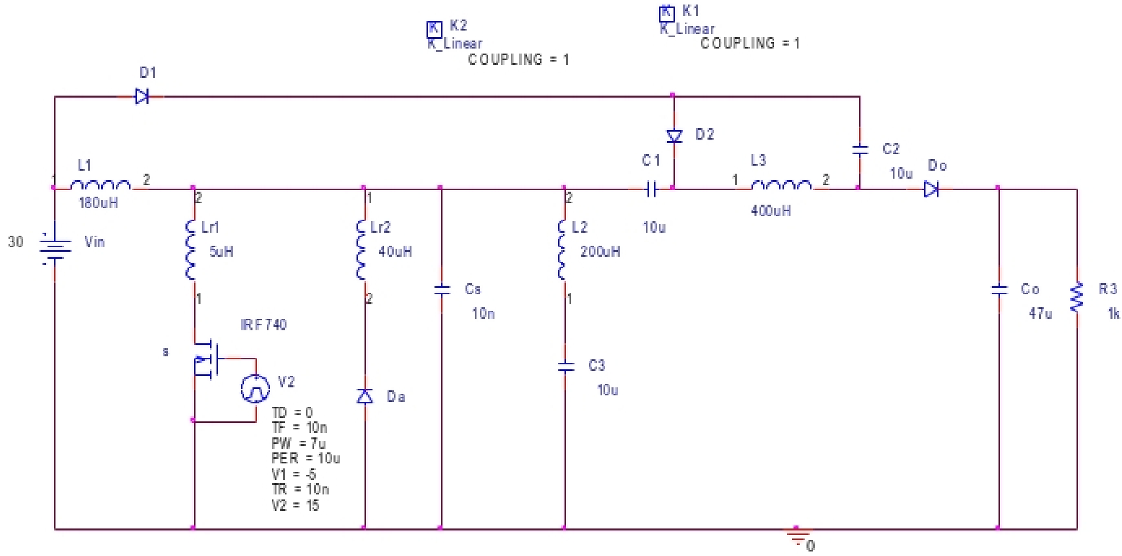


Fig. 8. Proposed converter circuit simulated in PSpice.

Table 1. Specifications of proposed converter and its elements values.

elements/specifications	part name/value
V_{in}	30 V
V_o	320 V
Power switch	IRF740
m	2.8
Turns ratio = N	1.4
L_{r1}	5 μH
C_1-C_3	10 μF
C_o	47 μF
C_S	10 nF
P_o	100 W
f_S	100 kHz

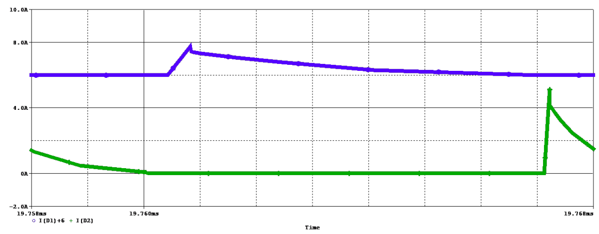


Fig. 10. Proposed converter diode D_1 (top) diode D_2 (bottom) current simulated waveforms in scale 2 A/div, 1 μs.

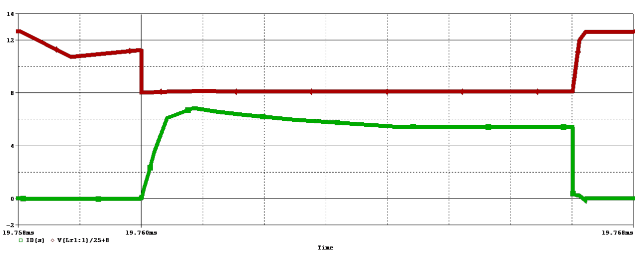


Fig. 9. Proposed converter switch simulated voltage and current waveforms in scale 2 A/div, 50 V/div, 1 μs.

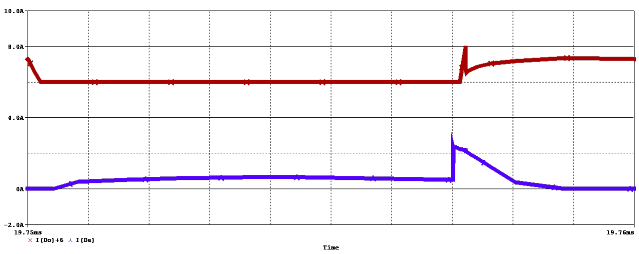


Fig. 11. Proposed converter diode D_o (top) diode D_a (bottom) simulated current waveforms in scale 2 A/div, 1 μs.

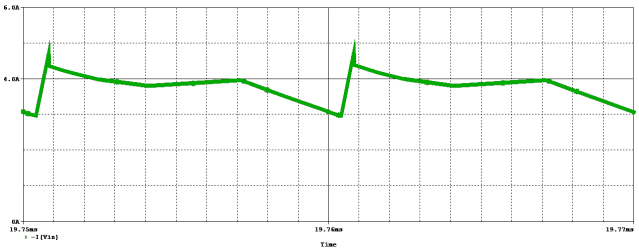


Fig. 12. Proposed converter input current simulated waveforms in scale (1 A/div, 1 μs)**.**

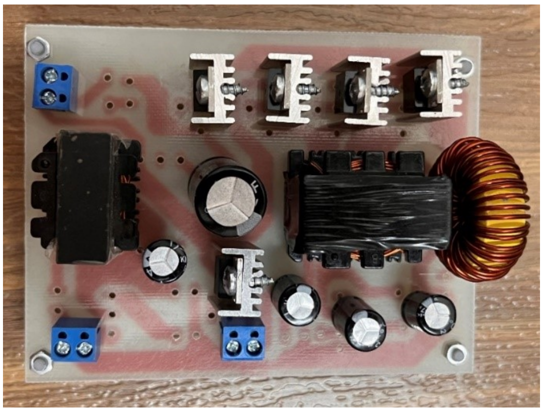
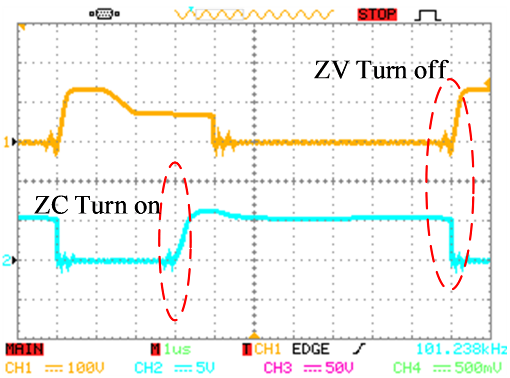
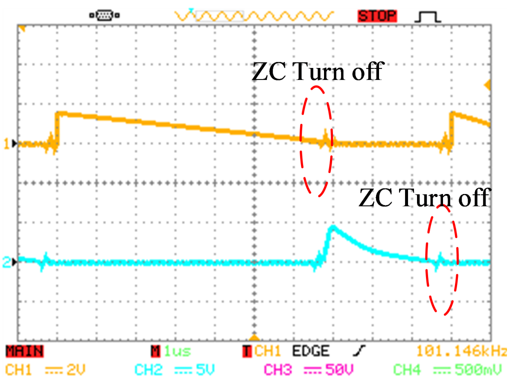


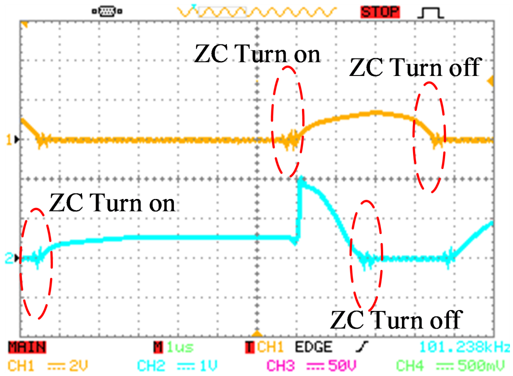
Fig. 13. The implemented converter.



(a)



(b)



(c)

Fig. 14. Practical waveforms of the semiconductor elements in the proposed converter. (a) Voltage (up) and Current (bottom) of the switch. (b) Current of diode D_1 (up) and current of D_2(bottom) (c) Current of diodes D_o (up) and current of D_a (bottom).

5 Comparison of Proposed Converter Efficiency with Proposed Converter without Auxiliary Circuit

Figure 15 shows the efficiency of the proposed converter. As observed, the highest efficiency of 95 percent is achieved at full load, and based on the converter design, the efficiency slightly decreases at lighter loads. If an RCD snubber is used instead of the auxiliary circuit (as shown in Figure 16), the full-load efficiency will decrease by 5% due to resistive losses and switching losses in the switch.

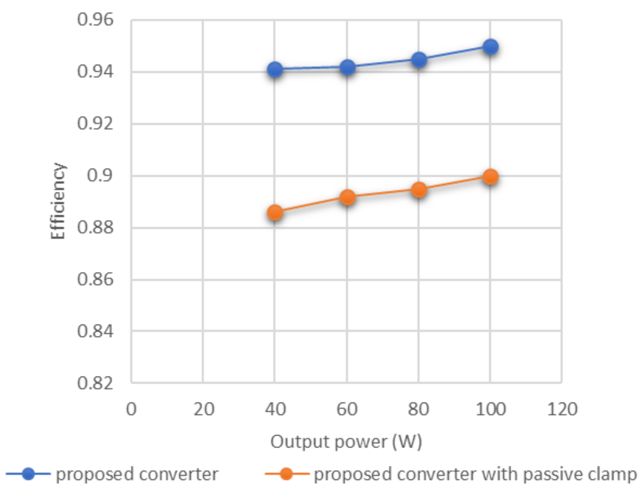


Fig. 15. Comparison of the efficiency diagram of the proposed converter with that of the proposed converter with passive clamp circuit.

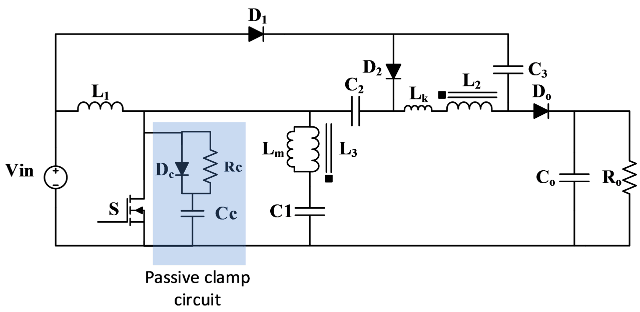


Fig. 16. The converter with passive clamp circuit

6 Comparison of Proposed Step-Up Converter with Previous Similar Converters

In this section, the performance of the proposed converter is compared with that of similar previous converters in terms of voltage gain, switch stress, switching characteristics, input current ripple, and component count, as presented in Table 2. Figure 17 displays the comparative voltage gain characteristics of these converters at a turn ratio of 2. As shown, the proposed converter, along with converter [20], achieves a higher voltage gain compared to converters [16] and [18], resulting in lower voltage stress. While converter [19] offers a higher voltage gain than the proposed converter, it operates with hard switching, leading to switching losses that reduce efficiency and power density. Furthermore, the higher input current ripple in converter [19] could potentially shorten the lifespan of the fuel cell in fuel cell-based systems.

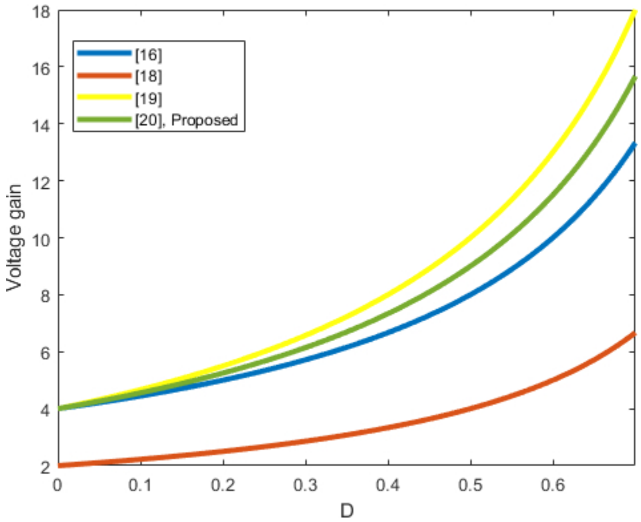


Fig. 17. The proposed converter voltage gain in comparison with similar converters.

Table 2. The comparison of accomplishing the converters and the proposed structure.

Converter	Voltage gain	Maximum voltage of switch	soft switching	Input current ripple	Number of				
					MC*	SW	D	C	T†
[16]	$\frac{n+2}{1-D}$	$\frac{V_o}{n+2}$	ZCS	Low	3	1	3	4	11
[18]	$\frac{n}{1-D}$	$\frac{V_o}{n}$	ZVS	Low	2	2	2	4	10
[19]	$\frac{n+2+nD}{1-D}$	$\frac{V_o}{n+2+nD}$	Hard	High	1	1	4	5	11
[20]	$\frac{n+2+D}{1-D}$	$\frac{V_o}{n+2+D}$	Hard	Low	2	1	4	6	13
proposed	$\frac{n+2-D+nD}{1-D}$	$\frac{V_o}{n+2-D+nD}$	ZCS	Low	2	1	4	5	12

*Magnetic core
†Total

7 Conclusion

This study presents a high step-up non-isolated converter that does not use a coupled inductor at the input. Instead, the auxiliary circuit uses a small coupled inductor, which, due to its small size, has very low leakage inductance, preventing unwanted resonance without increasing the volume and weight of the circuit. The proposed converter offers several advantages, including zero-current switching of the main switch during turn-on and zero-voltage switching during turn-off. It features low input current ripple due to the absence of a coupled inductor at the input, eliminates reverse recovery issues in the diodes, and reduces voltage stress on the switch. Additionally, it requires simple PWM control, does not need an auxiliary switch, provides very high voltage gain, and has a low component count in the auxiliary circuit. However, the main drawbacks of the converter are the high voltage stress on the output diode and the presence of capacitive turn-on losses in the switch. In the future, reducing the voltage stress on the output diode and minimizing capacitive turn-on losses in the switch will be important areas to address in order to improve the converter's performance and efficiency.

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